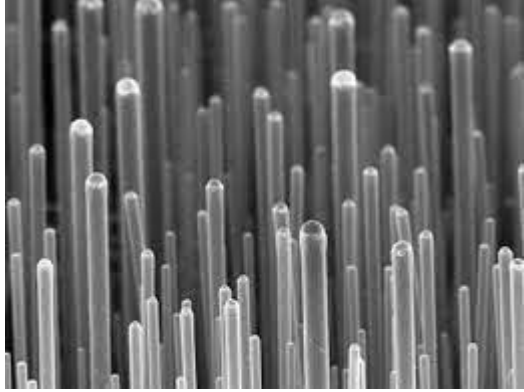
# Lesson 12:
# Vapor-Liquid-Solid Growth of Nanowires
# (The VLS mechanism; Role of the surface energies; Role of the size-dependent effects; Role of the phase diagrams and eutectic point; Growth equations; Lenght-radius dependence; Temperature conditions in the VLS mechanism; Experimental data and focus on semiconductor nanowires (Si, Ge); Solid-Liquid-Solid synthesis of one-dimensional nanostructures)

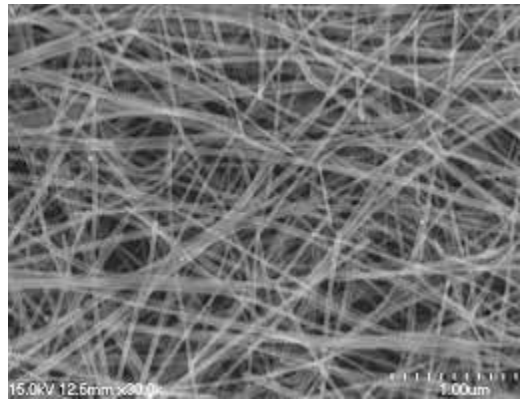
A nanowire is generally defined as an object with a one-dimensional aspect in which the ratio of the length to the width is greater than 10 and the width does not exceed a few tens of nanometers. Today, this definition has been extended to atomic and molecular wires, which have proved to exhibit very interesting physical properties without necessarily having the geometrical characteristics defined earlier.

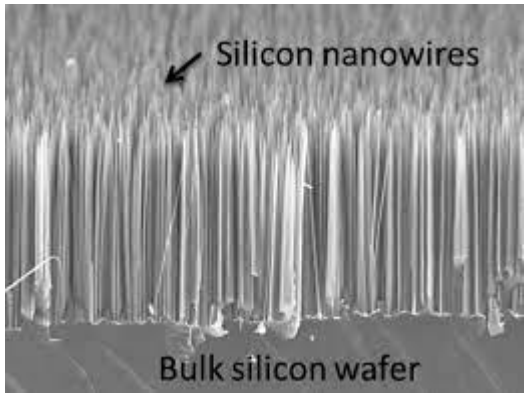
There are many potential applications for nanowires. However, nanowires can be divided into two categories:

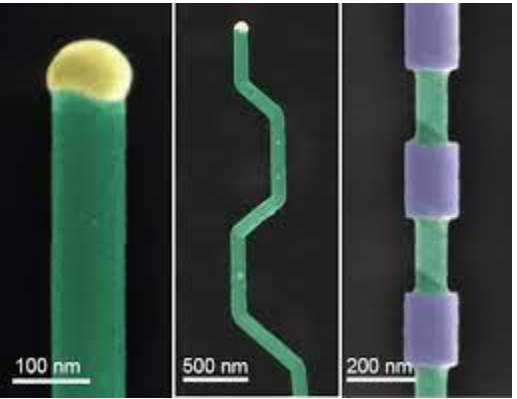
- nanowires with direct applications determined by their physical properties,
- nanowires used as basic building blocks in more complex devices.

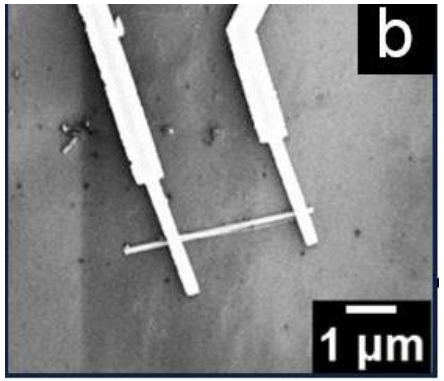
The direct applications mainly concern information storage, electronics and optronics. Examples are magnetic nanowires, light-emitting nanowires, or nanowires behaving as diodes. As elementary building blocks, nanowires are mainly used as electrical contacts, or as integral parts of components when they have semiconducting properties.

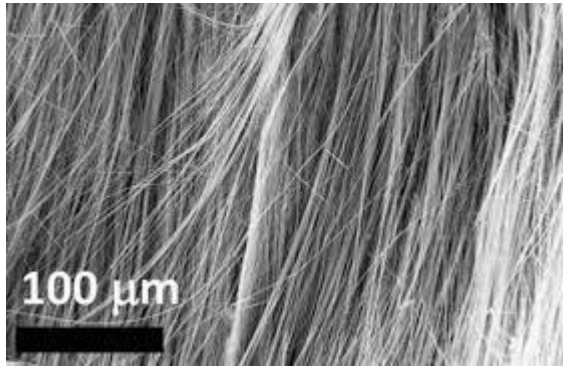






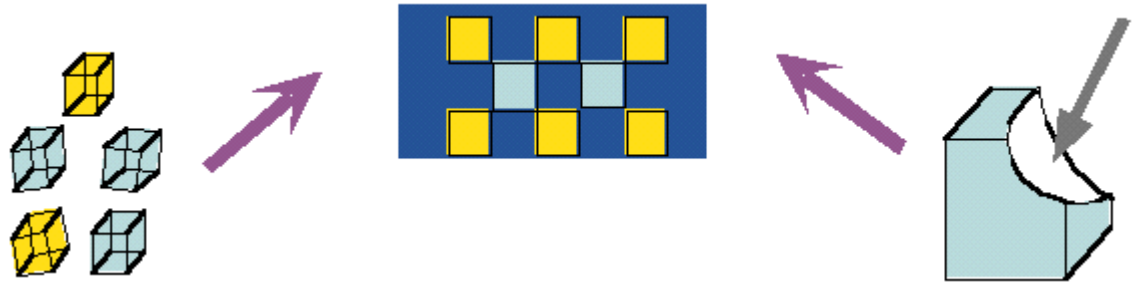



But whatever the application, nanowires are not yet an industrial product. Although there exist many ways of making them, the available methods do not yet combine mass production with very small dimensions. The subject

There are two distinct approaches to the fabrication of nanostructures: the top-down approach and the bottom-up approach, one arising in the world of microelectronics and the other in the world of nanophysics. Although the overall aim may be the same, i.e., to produce nanostructures in the broad sense of the term, the way of going about it is totally different in the two cases. Huge resources are invested in developing techniques that can combine mass production and extremely high levels of resolution in the fabrication process, in order to achieve what is known as nanotechnology. Unfortunately, at the present time, no technique can really achieve this, and some prefer to stay with the term nanoscience.

In the top-down approach, one attempts to reduce the size of a complex object to the point where this scale reduction begins to alter the very principles it is based upon. The idea is seductive at first glance, but this method encounters major physical and technological difficulties when one attempts to go down to length scales of a few tens of nanometers using conventional lithographic methods. When these targets are reached, using emerging lithographic techniques, one has to face the problem of speed: the slow production rate is quite incompatible with the requirements of mass production.

- Top-down



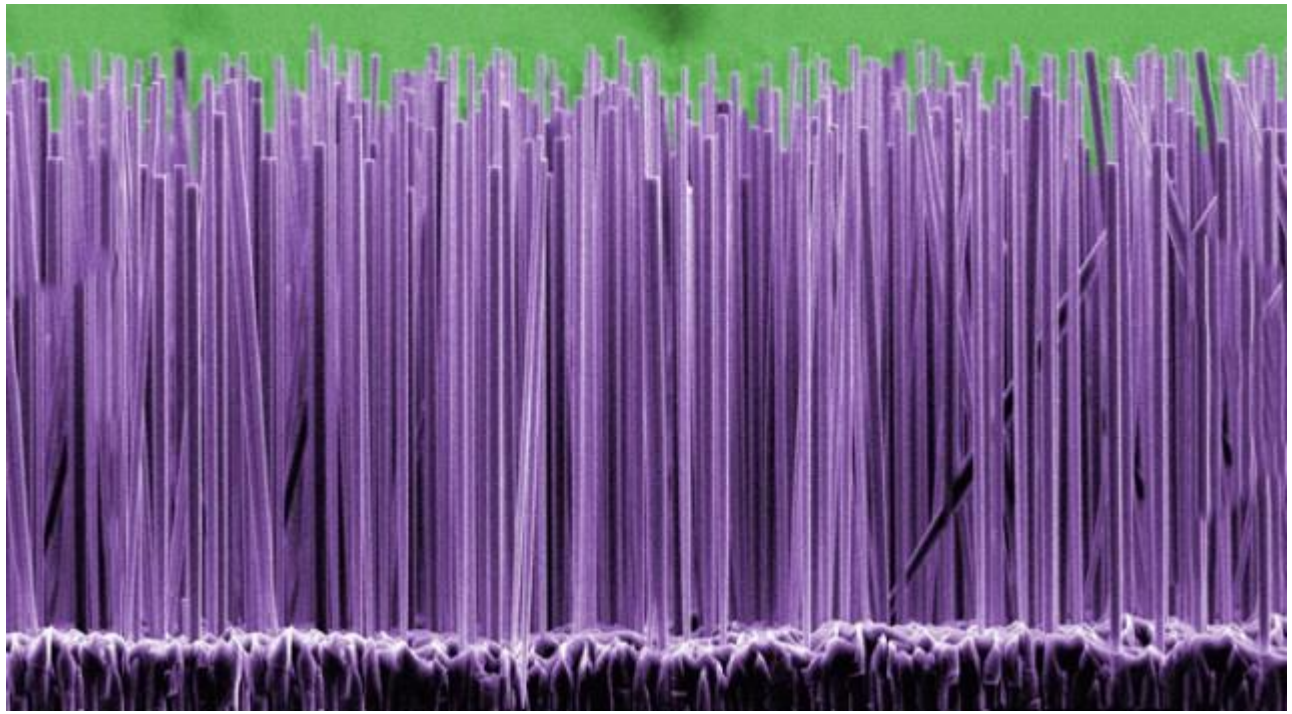
- Bottom-up

The bottom-up approach is radically different, since it involves using atomic scale and nanoscale physicochemical phenomena to fabricate simple nanostructures in a spontaneous manner and in large quantities. The resources required in this case are considerably reduced since growth and assembly can be controlled in a single step, and in a natural and self-regulating manner. This control over crystal growth can be used to fabricate identical objects with the same properties, and at an incomparably lower cost. The disadvantage of this approach is that transistors, memory cells, and other components do not a priori form in a spontaneous way. The bottom-up approach thus requires the invention and study of new components compatible with this means of fabrication. This is why many specialists say that, if there is to be a revolution one day, it will necessarily be here.

Apart from lithographic techniques used in the microelectronics industry which we shall not be concerned with here, the work currently being carried out in the field of nanowire fabrication can be classified as follows:

1. Using a top-down approach:
   a) conventional high resolution lithographic techniques (electron beam, extreme UV, and X ray),
   b) alternative lithographic techniques:
      - nanoimprinting,
      - nanomoulding,
      - lithography by near-field microscopy,
2. Using a bottom-up approach:
   a) self-assembly techniques,
   b) VLS synthesis,
   c) use of porous matrices.

# VLS Synthesis



The VLS (vapour–liquid–solid) technique consists in growing nanowires from a molten droplet [40, 41]. This droplet is created in a high temperature reactor (around 900°C) and fed either by a vapour phase produced from a target bombarded by a laser, or by CVD, or both at once. The method is particularly well suited to the growth of semiconductors and metal alloys for which the phase diagrams can be perfectly controlled. Nanowires of diameter 10 nm and length several microns can be fabricated in this way. With this technique, it is also possible to vary the composition of the interior of the nanowire by controlling the composition of the vapour phase arriving on the droplet. It is then possible to make doped or undoped semiconducting nanowires (Si, GaAs, InP, GaN, etc.) or multilayer metallic nanowires with magnetic properties, and even to control to a certain extent the composition of the outer part of the wire. The growth of the wire is directly linked to the Gibbs–Thomson effect which shows that the smaller the diameter, the slower the growth will be (see Fig. 9.7).

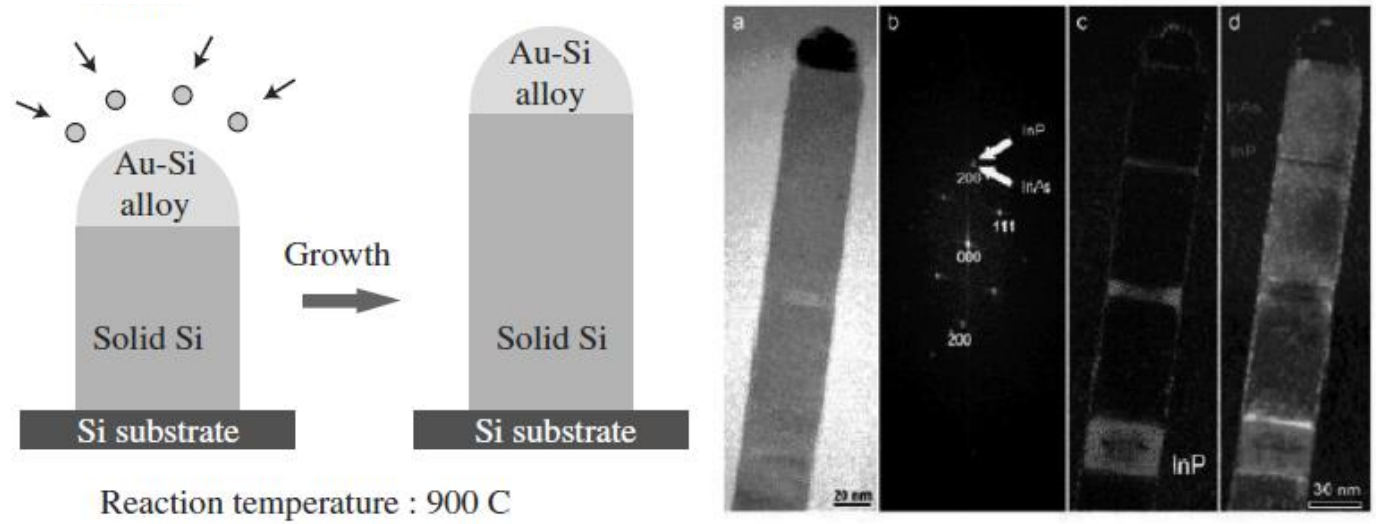



**Fig. 9.7.** VLS fabrication method. Image of a multilayer InAs/InP nanowire with diameter 30 nm. Courtesy of Karaguchi et al. [41]

Using the bottom-up VLS approach, nanowires with a typical radius of 10–100 nm and length up to several μm can be obtained by using modern epitaxy techniques such as MOCVD and MBE. Nanowire materials include elementary semiconductors Si and Ge [258–260, 281, 298], III-V [264, 265, 270–279], II-VI [282, 301] compounds and oxides [302]. VLS semiconductor nanowires are interesting for their unique physical properties, some of which are listed below:

(i) The growth mechanisms including a complex physical chemistry of liquid and solid alloys, 1D diffusion transport, specific features of nucleation in confined nano-volumes, droplet configurations, different non-stationary and non-linear growth effects;
(ii) The morphology including the control over length and radius uniformity, fabrication of spatially ordered nanowire arrays, and tunable nanowire shapes;
(iii) The crystal structure featuring surprising ZB-WZ polytypism of III-V nanowires, rotational twinning, developing methods to control the crystal phase during growth;
(iv) Dramatically enhanced role of surface effects leading, in particular, to a very efficient relaxation of elastic stress on free sidewalls and enabling coherent growth of epitaxial nanowires on lattice mismatched substrates;
(v) Synthesis methods and physical properties of axial and core-shell heterostructures in nanowires, including elastic relaxation and structural defects;
(vi) The doping processes and the formation of p-n junctions in nanowires;
(vii) Transport and optical properties, including those in nanowire heterostructures, with a variety of possible dimensions, morphologies and crystal structures and a possibility to realize single electron transport and single photon emission and detection.

As for applications, semiconductor nanowires show great promise as the key elements for field effect transistors [260, 267, 277, 283], high electron mobility transistors [264], resonant tunneling diodes [273], single electron memory devices [279], high efficiency light emitters [265, 274], solar cells [281], sensors [262, 266]

In simple terms, the VLS method utilizes the catalytic effect of a metal droplet which is liquid during growth. The droplet promotes the vertical nanowire growth and defines the nanowire position and radius, while the nanowire length is roughly proportional to the deposition time. Let us first discuss qualitatively the physical nature of the VLS growth during chemical vapor deposition (CVD) according to Wagner and Ellis [46] and Givargizov [47]. The process is illustrated in Fig. 4.2 In the 1960–1970s, typical CVD growth temperatures of Si from $SiCl_4$ and $H_2$ on silicon substrates were above 1100 °C. By decreasing the substrate temperature to 1000 °C or lower, one could therefore almost completely avoid the surface growth. The (111) substrate orientation was chosen for two reasons: the lowest rate of 2D growth and, more importantly, the preferred $< 111 >$ wire growth orientation where the wires are perpendicular to the (111) substrate. The Si(111) substrates were activated by Au droplets, which can be accessed by simply depositing a thin solid Au layer and then annealing it before turning on a Si source. The annealing temperature as well as the VLS growth temperature must be higher than the eutectic melting temperature of the corresponding metal-semiconductor alloy (Au-Si in our example). Surprisingly, while bulk Au and Si themselves melt at 1064 °C and 1410 °C, respectively, the melting temperature of the Au-Si alloy is as low as 363 °C [306]. This value gives the lowest possible VLS growth temperature disregarding the size-dependent depression of the melting point. Since most of liquid metals do not wet semiconductor surfaces, the alloy segregates into an ensemble of spherical cap droplets.

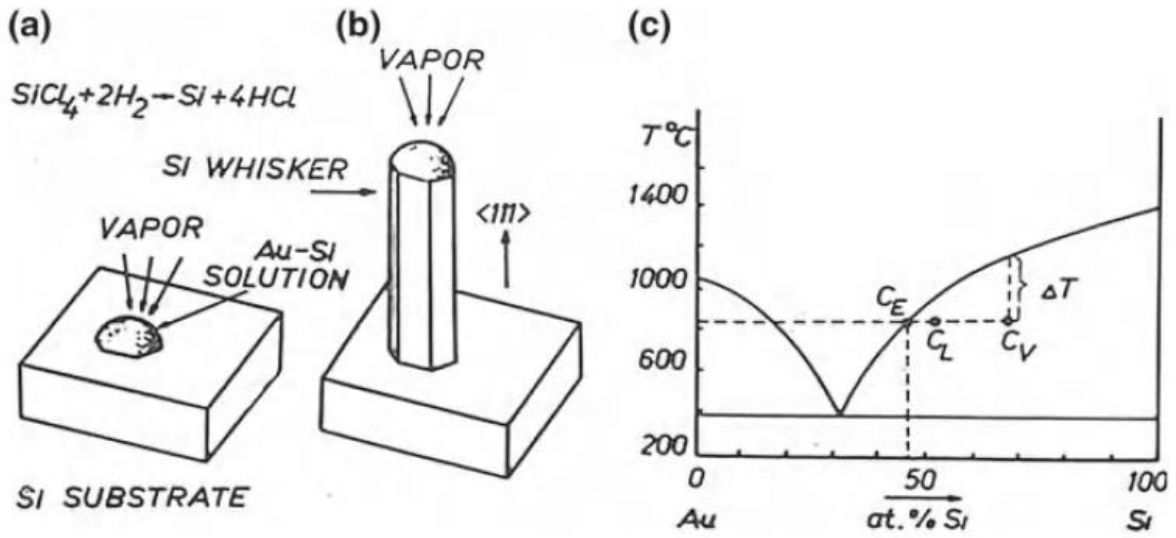
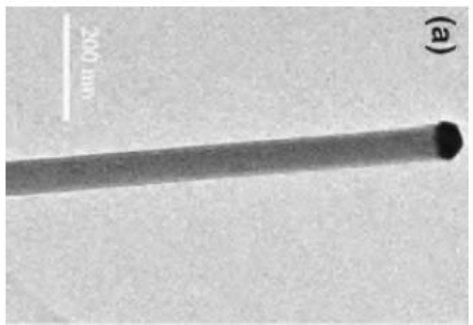



**Fig. 4.2** The Wagner-Ellis sketch schematizing the VLS growth of Si "whiskers" by the Au-assisted CVD [46]: **a** Au-Si droplet on the substrate surface; **b** whisker growth under the droplet; **c** Au-Si phase diagram showing the melting point at 363 °C and the equilibrium silicon concentration $C_E$ at the liquidus (*solid line*) at a given surface temperature $T$ (*dashed line*). Vapor flux renders the Si concentration in the alloy into a supersaturated value $C_L$; $\Delta\mu_{LS} = \mu(C_L) - \mu(C_E)$ is the difference of Si chemical potentials in the liquid and solid states, and $\Delta\mu_{VS} = \mu(C_V) - \mu(C_E)$ is the difference of Si chemical potentials in the vapor and solid states. Temperature $T + \Delta T$ corresponds to the point at which the entire VLS system would be in equilibrium

When Si precursor is supplied to the substrate, the pyrolysis reaction $SiCl_4 + 2H_2 \rightarrow Si + 4HCl$ takes place only at the droplet surface. Silicon either dissolves in the droplet or re-evaporates. However, more Si arrives from vapor than desorbs, thus creating a certain Si concentration in the Au-Si alloy ($C_L$) which is above its equilibrium concentration ($C_E$) at a given temperature($T$). On the other hand, $C_L$ is lower than the concentration ($C_V$) at which the arrival rate from vapor would be equalized by desorption to the vapor phase (which is at a different temperature). Liquid alloy in the droplet is rendered into a supersaturated value by the vapor influx and crystallizes at the liquid–solid interface under the droplet. The composition of the precipitated solid phase corresponds to that of the phase boundary and thus is pure Si according to the diagram. This crystallization usually proceeds via the nucleation and lateral extension of 2D islands, as in the conventional liquid phase epitaxy but in a laterally confined area. This leads to the nucleation-mediated vertical growth of a cylindrical solid rod under the droplet, whose radius is defined by the initial droplet size. In a steady state, the arrival of Si from vapor is exactly equalized by its sink due to the crystallization. Silicon is thus transformed from the vapor to the solid state via an intermediate liquid state by two consecutive phase transitions: the vapor-liquid condensation and the liquid–solid crystallization, which explains the term "vapor–liquid–solid" growth. The mechanism described above can be realized only when the vapor-solid difference of chemical potentials $\Delta\mu_{VS}$ is larger than the liquid–solid one $\Delta\mu_{LS}$ (the necessary condition for a positive vapor-liquid flux) and the latter is positive (the necessary condition for the liquid–solid flux). Here and below, we

Modern MOCVD and MBE techniques for the VLS nanowire synthesis use very similar growth strategy, illustrated in Fig. 4.3 in the case of Au-catalyzed MBE of GaAs wires on GaAs(111)B substrates. Although Au is the most common catalyst for Si, Ge and III-V nanowires, some other metals can also be utilized as discussed later on. The growth procedure usually includes four steps:

1. Substrate de-oxidation and growth of a GaAs buffer layer in the MBE growth chamber.
2. Deposition of ~1 nm thin Au film in an ultra-high vacuum chamber or a metallization chamber which is placed inside the vacuum part of MBE machine but is separated from the growth chamber in order to avoid the unwanted Au contamination.
3. Anneal of Au above the eutectic melting temperature with Ga (usually around 600 °C) in the MBE growth chamber in order to form the equilibrium droplets. This simple procedure always results in a broad size distribution, with typical examples shown in Fig. 4.4. Under the identical annealing conditions, larger equivalent thickness of Au layer leads to a large mean size and a wider size distribution.
4. MBE deposition of GaAs above the eutectic temperature resulting in the VLS nanowire growth. The growth process can be performed under different conditions such as the substrate temperature (usually in the range of 500–600° for GaAs), Ga deposition rate, $As_2$ or $As_4$ flux, and deposition thickness. Together with the initial size distribution of Au droplets, these conditions influence the resulting nanowire morphology: radii, lengths, surface density and shapes.



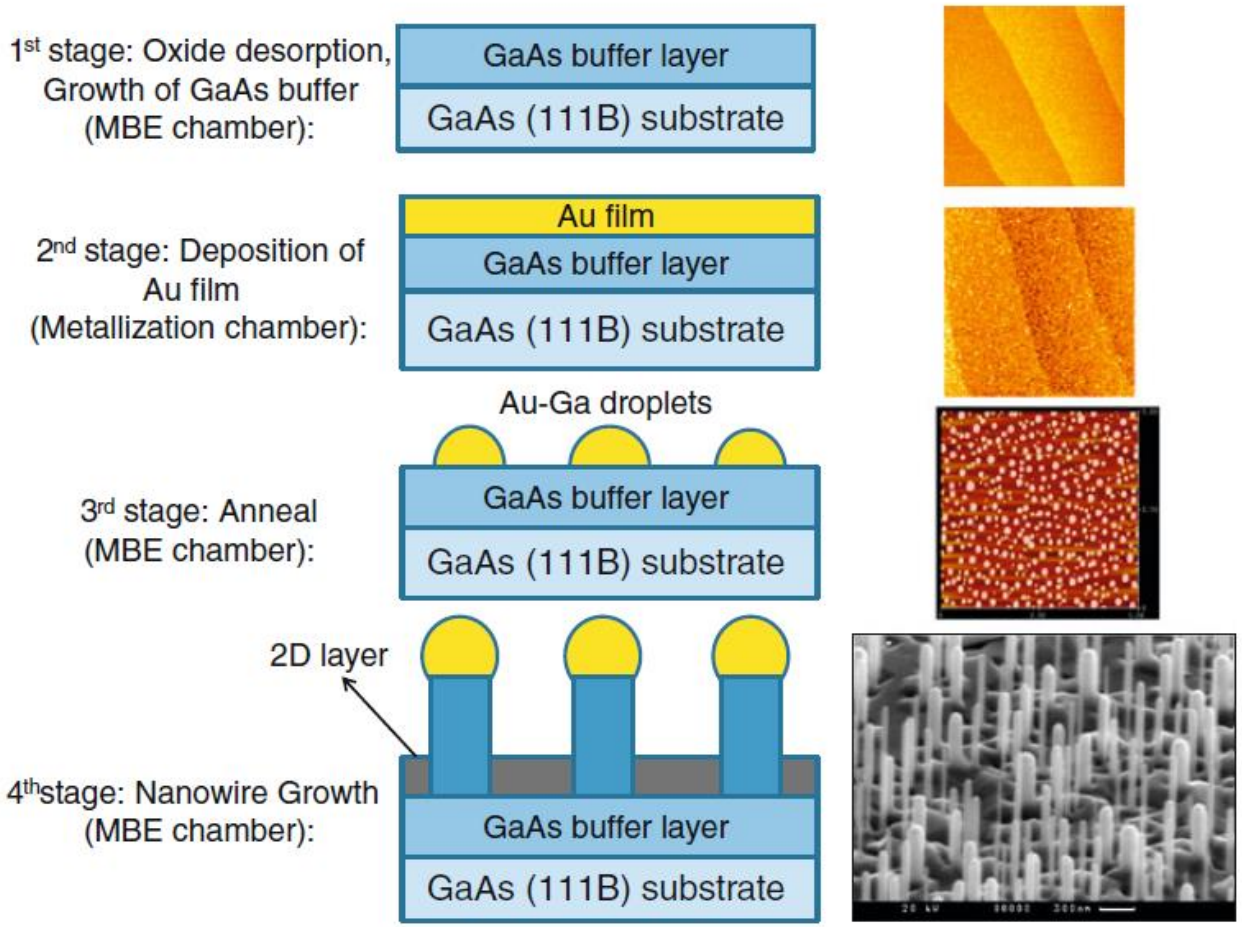
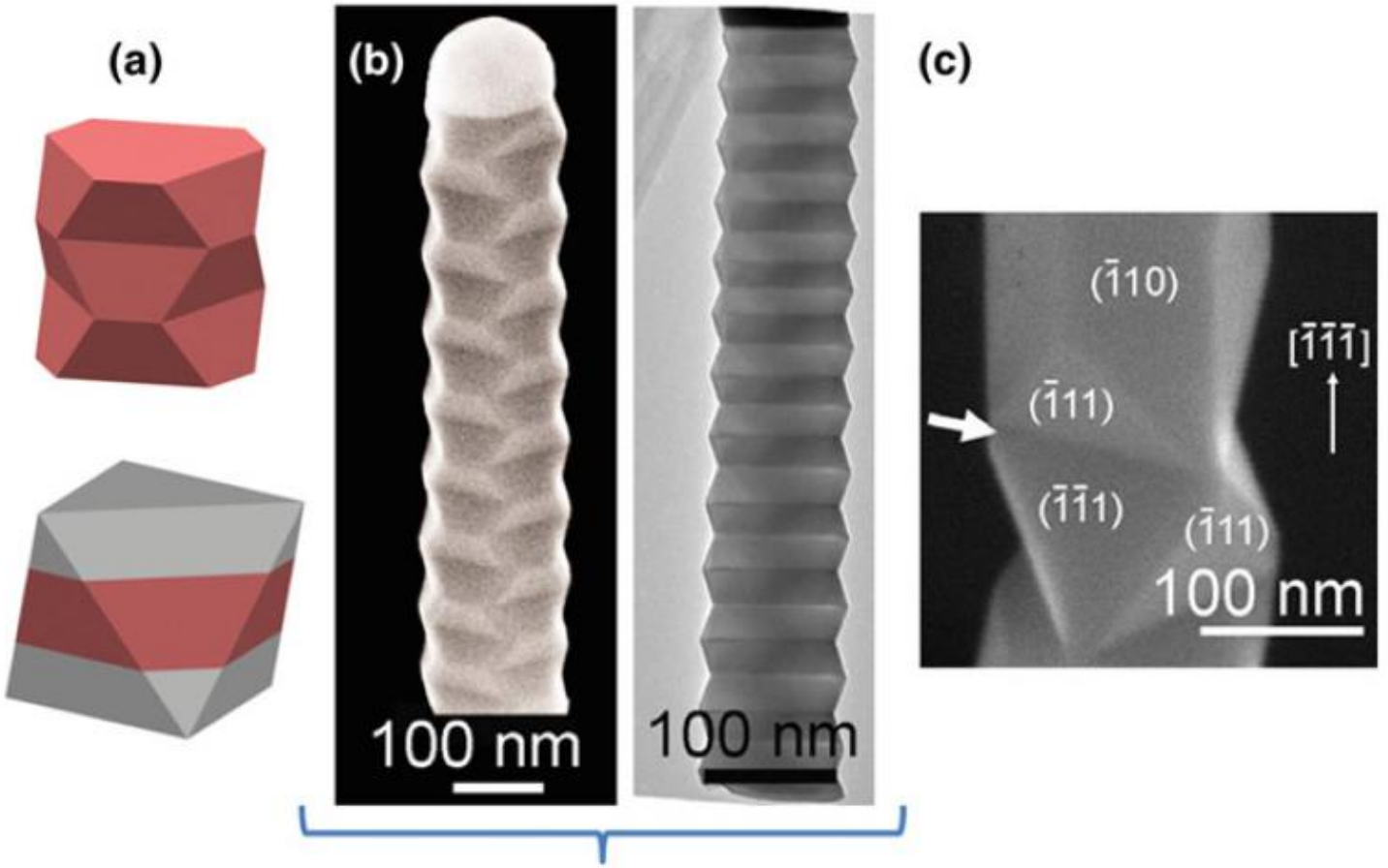




**Fig. 4.3** Au-assisted VLS growth of GaAs nanowires on GaAs(111)B substrate by MBE, AFM images show the GaAs buffer (1st stage), the surface after Au deposition (2nd stage), 3D droplets after annealing (3rd stage), and SEM image shows the vertically aligned GaAs wires (4th stage)




Twinning

**Fig. 4.6** **a** 3D model of a twinned nanowire with (111) microfacets. The octahedral slice is cut from the middle part of the full octahedron. **b** Examples of InAs nanowires from [234] exhibiting this facet structure are shown by SEM (left) and TEM (right). The height of the section varies with growth conditions up to the limit case of the full octahedron. **c** SEM image of an InAs nanowire containing a full octahedron, with some of the (111)-type facets labelled. The *thick arrow* indicates the twin plane following an octahedron. Above the octahedron, the side facets convert to the (110) type. These InAs nanowires were grown by MOCVD with aerosol Au nanoparticles as the growth seeds at temperatures above 400 °C [234]

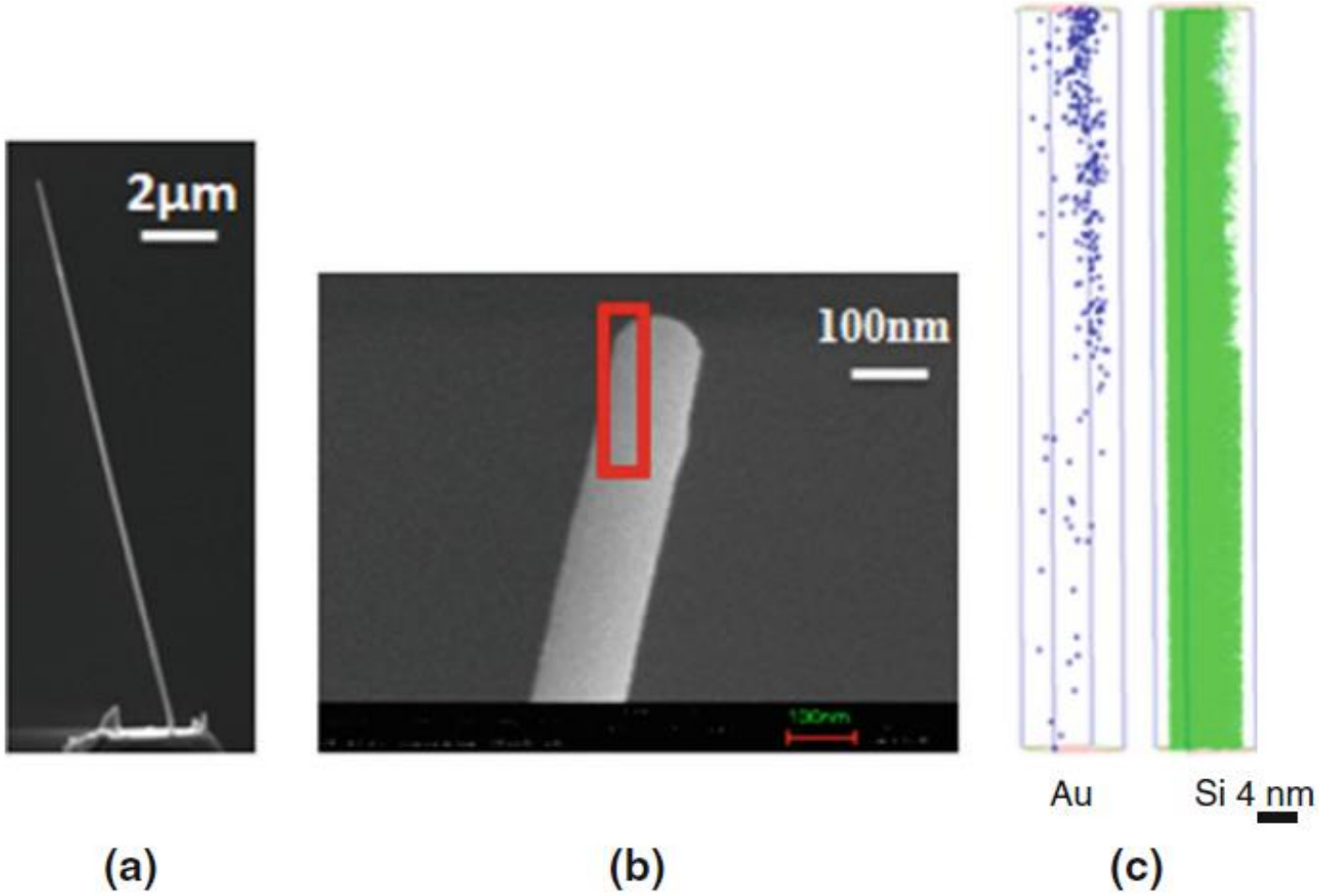



**Fig. 4.11** **a** SEM image of an Au-catalyzed Si wire grown on a Si micropillar for APT measurements. **b** Magnified image showing the investigated region. **c** Atomically resolved 3D APT reconstruction of Au and Si distributions in the sidewall region under the droplet

# Metal Catalyst Contamination

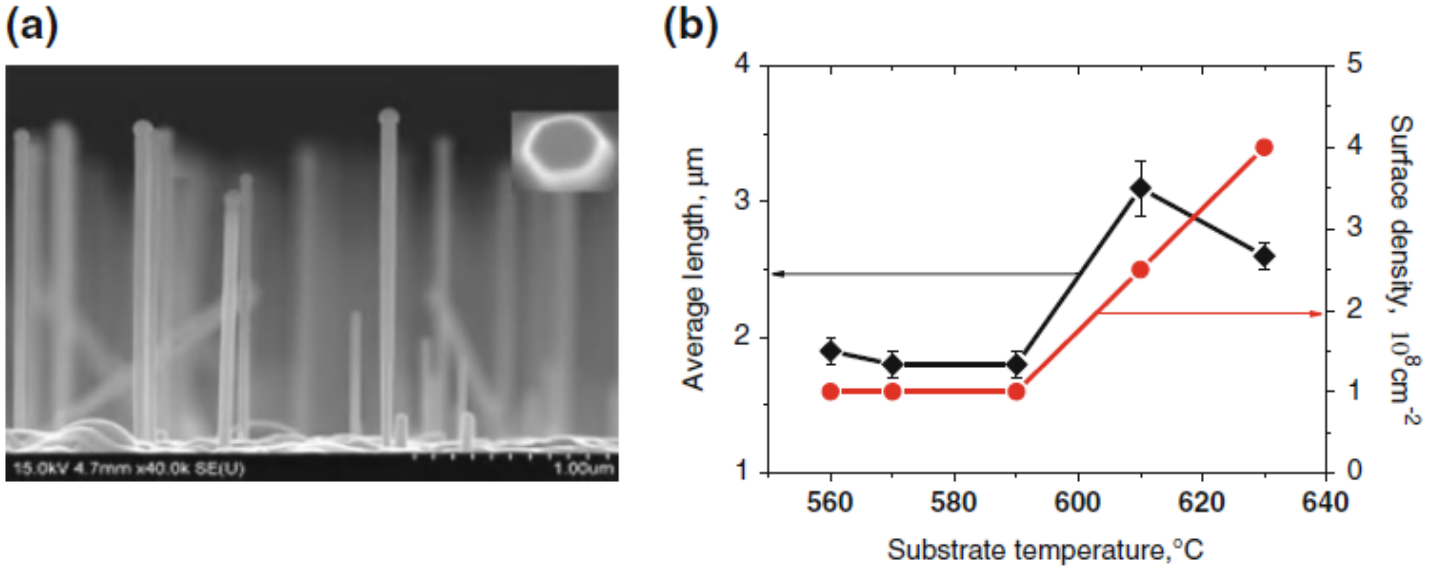



**Fig. 4.12** **a** Lateral cross-section view SEM image of Ga-catalyzed GaAs nanowires on Si(111) substrate grown at 590 °C, the *inset* shows the hexagonal nanowire cross-section. **b** Substrate temperature dependences of the average length and surface density

# Versatility

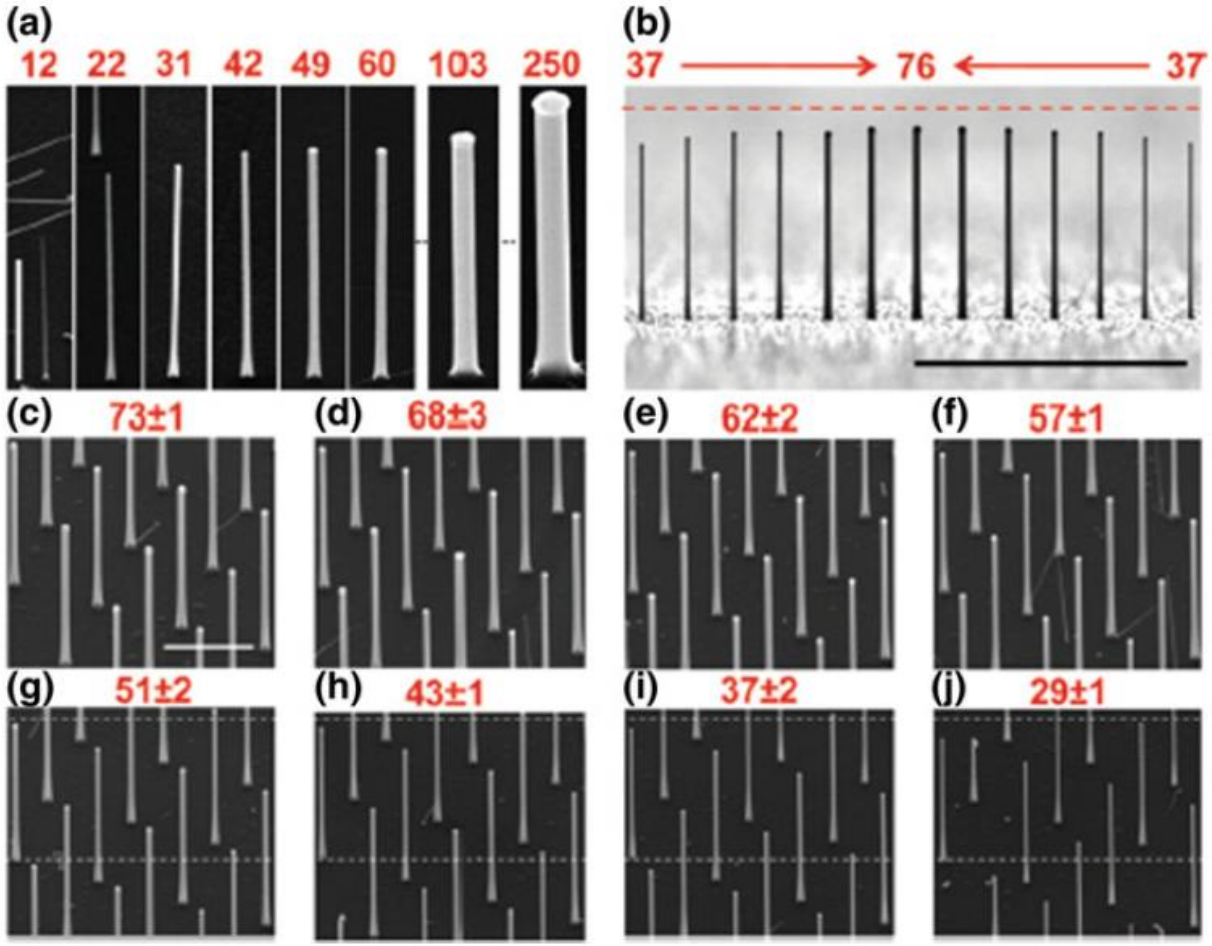



**Fig. 4.19** Ge nanowires with controllable diameter. **a** SEM images of vertical nanowires grown for 15 min at 276 °C from randomly dispersed Au colloids of nominal diameter 10, 20, 30, 40, 50, 60, 100, and 250 nm. The resultant measured average nanowire diameter (nm) is indicated at the *top* of each SEM image. The images were taken at the same magnification and the angle-corrected scale bar (far left side, vertical bar) is 1.41 μm. **b** Linear array of Ge nanowires grown from lithographically patterned Au *dots*. The *dashed red line* highlights the systematic changes in nanowire length at different diameters. Scale bar is 3 μm. **c–j** Arrays of uniformly sized Ge nanowires grown from Au *dots* with 100, 90, 80, 70, 60, 50, 40, and 30 nm diameter, 20 nm thickness, and 1 μm spacing, grown for 10 min at 276 °C. The resulting average nanowire diameters and statistical standard deviations are indicated at the *top* of each SEM image. Scale bar is 1 μm. The *dashed white lines* in (**e–h**) serve as a guide-to-the-eye for comparing the left-most nanowire lengths [376]

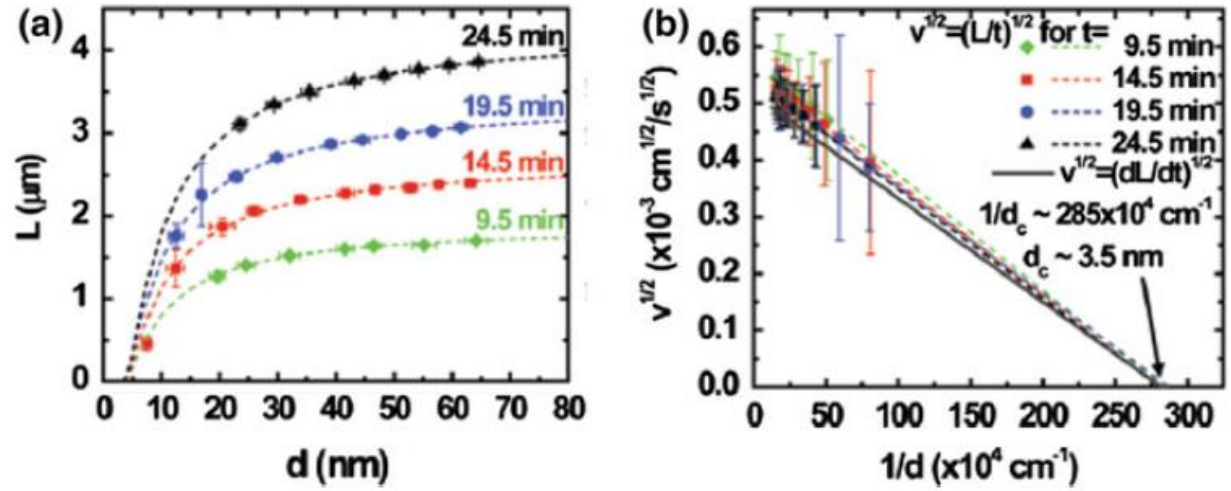



**Fig. 4.20** Plots of Ge nanowire growth rate with and without doping illustrating applicability of the Gibbs-Thomson effect on their growth. **a** Plot of the nanowire length as function of diameter with a P[GeH4] = 0.6 Torr for different growth times at the low temperature step (276 °C) = 5, 10, 15, and 20 min, resulting in a linear increase of length with time for all diameters. **b** Plot of the square root of the growth velocity for the data shown in **a** calculated using *L/t* and *dL/dt* showing convergence of all data to the same cutoff diameter of ~3.55 nm

Regardless of the epitaxy technique used for material deposition, modern VLS growth methods are characterized by the following general features:

- Appropriately optimized growth conditions usually enable close to 100 % yield of vertical wires.
- Position and surface density of VLS nanowires are determined by the properties of the initial ensemble of metallic droplets.
- The nanowire radius is determined by the size of initial droplet, while the nanowire length depends on the deposition conditions, growth time and the nanowire radius.
- VLS growth from the size-uniform and spatially ordered arrays of droplets results in the regular arrays of exactly identical nanowires.

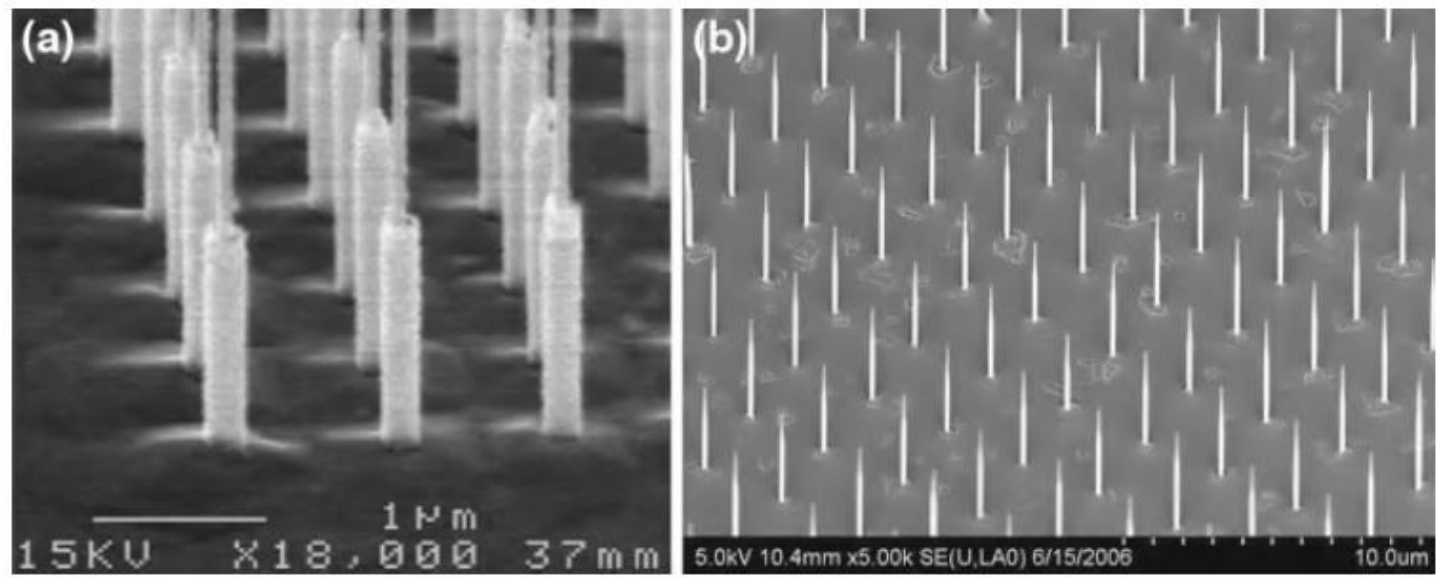



**Fig. 4.13** Regular arrays of Au-catalyzed InAs (**a**) [332] and GaAs (**b**) nanowires

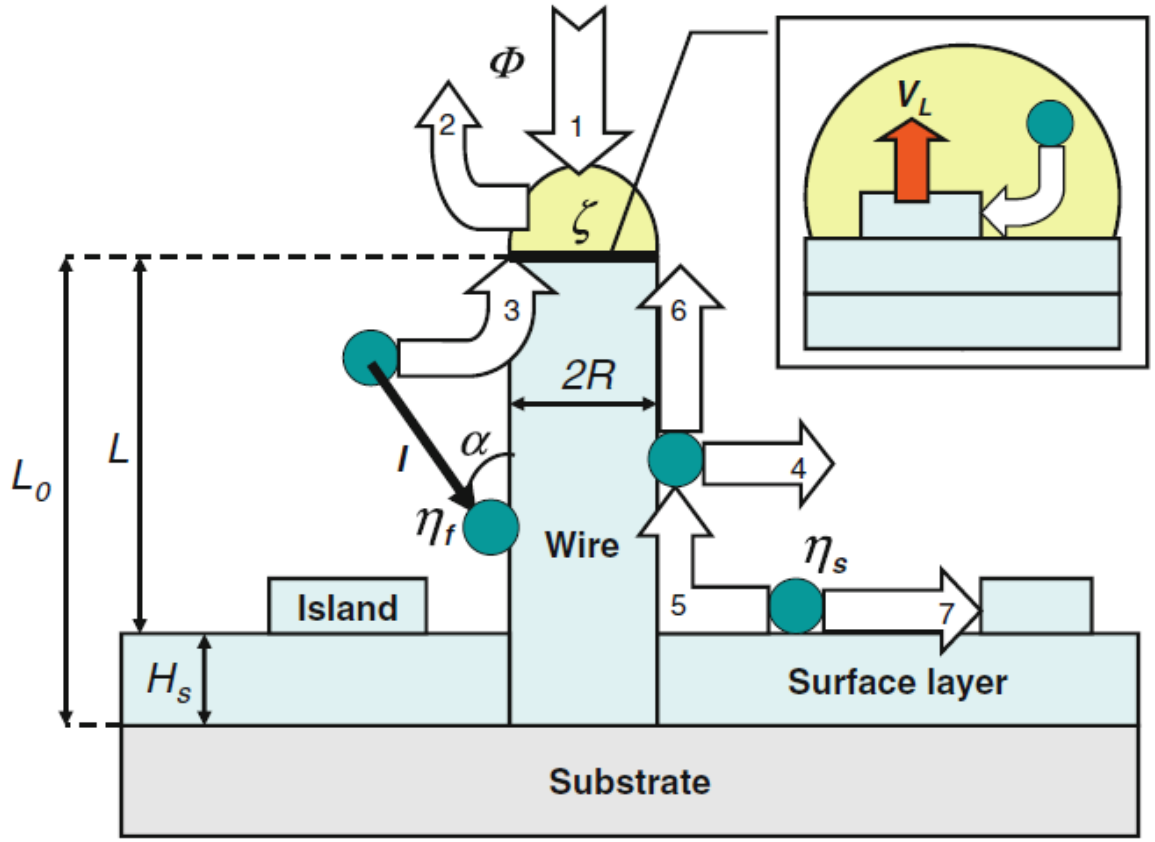



**Fig. 4.15** Kinetic processes during the VLS nanowire growth: *1*—direct impingement onto the droplet surface; *2*—desorption from the droplet, *3*—diffusion flux from the sidewalls to the droplet, *4*—desorption from the sidewalls, *5*—diffusion from the substrate to the sidewalls, *6*—diffusion from the substrate along the sidewalls to the drop, *7*—nucleation on the surface. The insert shows the nucleation-mediated growth on crystal facet under the drop, resulting in the vertical growth rate $V_L = dL_0/dt$. The wire length $L = L_0 - H_s$, where $H_s$ is the mean thickness of a 2D surface layer burying the wire bottom

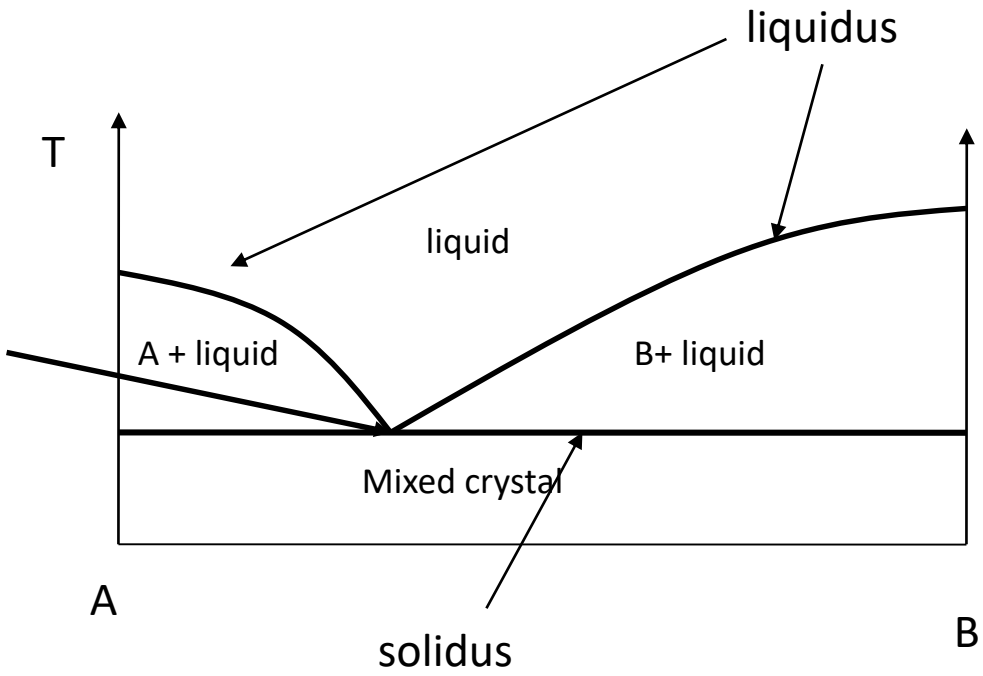
Adequate theoretical modeling of the VLS nanowire growth should therefore include:

- The mass transport equations describing different kinetic pathways to the droplet;
- Modeling of droplet configurations and stability depending on the material parameters and the growth conditions;
- Description of 2D nucleation process at the liquid–solid interface or at the triple phase line;
- Accounting for the size-dependent effects such as the Gibbs-Thomson effect, the mononuclear growth and the position-dependent nucleation rate;
- Self-consistency in the steady state VLS process implying that the nucleation-mediated vertical growth rate equalizes the total material flux into the droplet;
- Modeling of material and kinetic parameters entering the growth equations: chemical potentials in the droplet, surface energies of different interfaces, diffusion lengths etc.

# Eutectic:

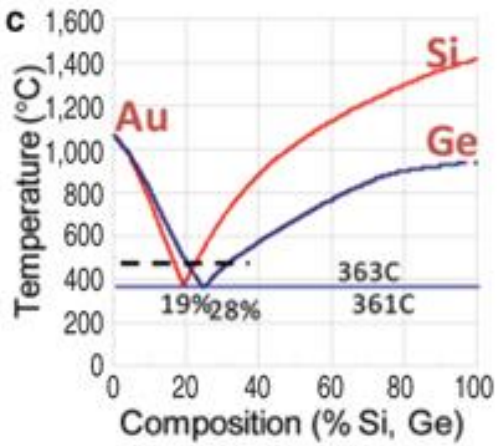
- coexistence of **3** phases
- lowest temperature where system is still totally liquid
- minimum of liquidus curve
- solid in solid + liquid phase consists of only one material

Eutectic

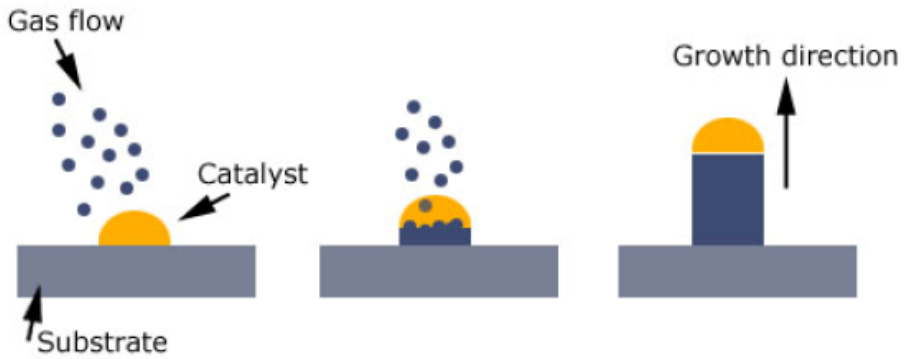



- mix of semiconductor and metal
- eutectic
- melting point of Semiconductor with metal lower - growth of one pure material

→ metal as catalyst




Spontaneous Growth,
**Vapor Liquid Solid Growth (VLS)**




Growth species in the catalyst droplets subsequently precipitates at the growth surface resulting in the ***one-directional growth***

# VLS: critical diameter, so that the liquid catalyst clusters are stable in equilibrium

The materials system used, as well as the cleanliness of the vacuum system and therefore the amount of contamination and/or the presence of oxide layers at the droplet and wafer surface during the experiment, both greatly influence the absolute magnitude of the forces present at the droplet/surface interface and, in turn, determine the shape of the droplets. The shape of the droplet, i.e. the contact angle ($\beta_0$, see Figure 4) can, be modeled mathematically, however, the actual forces present during growth are extremely difficult to measure experimentally. Nevertheless, the shape of a catalyst particle at the surface of a crystalline substrate is determined by a balance of the forces of surface tension and the liquid–solid interface tension. The radius of the droplet varies with the contact angle as:

$$R = \frac{r_o}{\sin(\beta_o)},$$

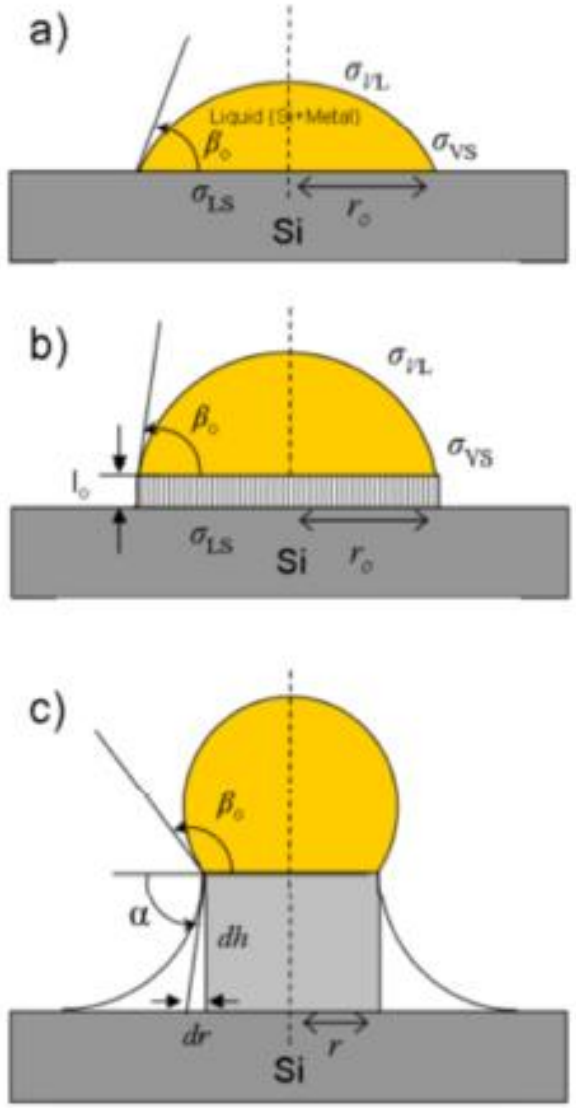
where $r_0$ is the radius of the contact area and $\beta_0$ is defined by a modified Young's equation:

$$\sigma_1 \cos(\beta_o) = \sigma_s - \sigma_{ls} - \frac{\tau}{r_o},$$

It is dependent on the surface ($\sigma_s$) and liquid–solid interface ($\sigma_{ls}$) tensions, as well as an additional line tension ($\tau$) which comes into effect when the initial radius of the droplet is small (nanosized). As a nanowire begins to grow, its height increases by an amount *dh* and the radius of the contact area decreases by an amount *dr* (see Figure 4). As the growth continues, the inclination angle at the base of the nanowires ($\alpha$, set as zero before whisker growth) increases, as does $\beta_0$:

$$\sigma_1 \cos(\beta_o) = \sigma_s \cos(\alpha) - \sigma_{ls} - \frac{\tau}{r_o}.$$

The line tension therefore greatly influences the catalyst contact area. The most import result from this conclusion is that different line tensions will result in different growth modes. If the line tensions are too large, nanohillock growth will result and thus stop the growth.

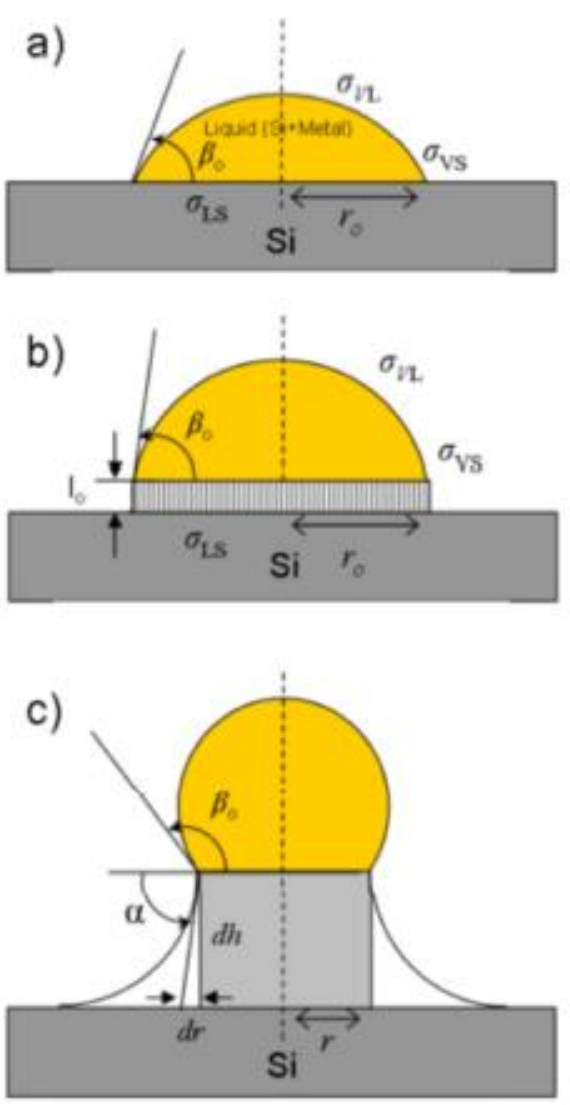


# Nanowhisker diameter

The diameter of the nanowire which is grown depends upon the properties of the alloy droplet. The growth of nano-sized wires requires nano-size droplets to be prepared on the substrate. In an equilibrium situation this is not possible as the minimum radius of a metal droplet is given by[4]

$$R_{\min} = \frac{2V_l}{RTln(s)}\sigma_{lv}$$

where $V_l$ is the molar volume of the droplet, $\sigma_{lv}$ the liquid-vapor surface energy, and $s$ is the degree of supersaturation[5] of the vapor. This equations restricts the minimum diameter of the droplet, and of any crystals which can be grown from it, under typically conditions to well above the nanometer level. Several techniques to generate smaller droplets have been developed, including the use of monodispersed nanoparticles spread in low dilution on the substrate, and the laser ablation of a substrate-catalyst mixture so to form a plasma which allows well-separated nanoclusters of the catalyst to form as the systems cools.[6]




$s=C/C_\infty$

C = concentration of semiconductor component in liquid alloy

$C_\infty$ = equilibrium concentration

# Solid-Liquid-Solid (SLS) synthesis of 1D nanostructures

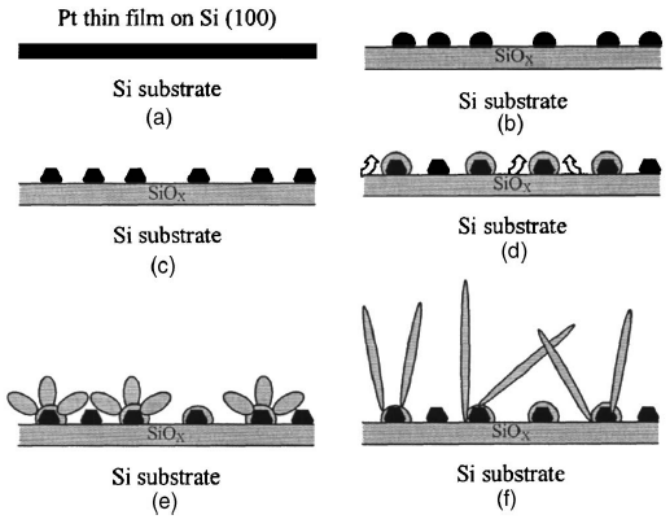
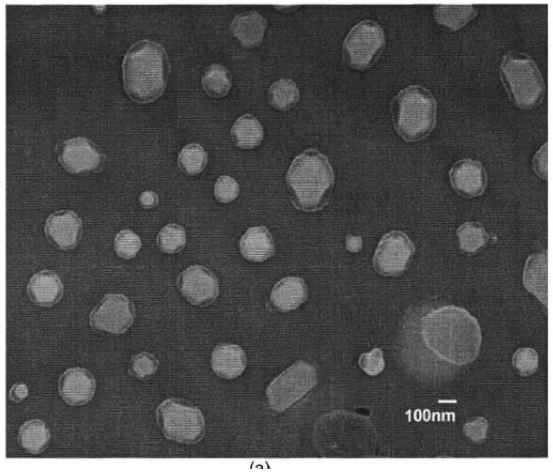
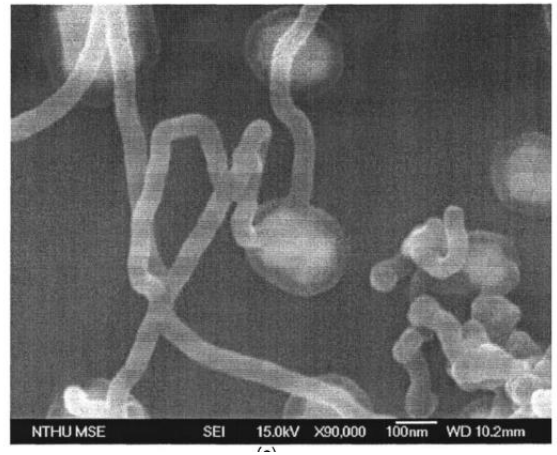
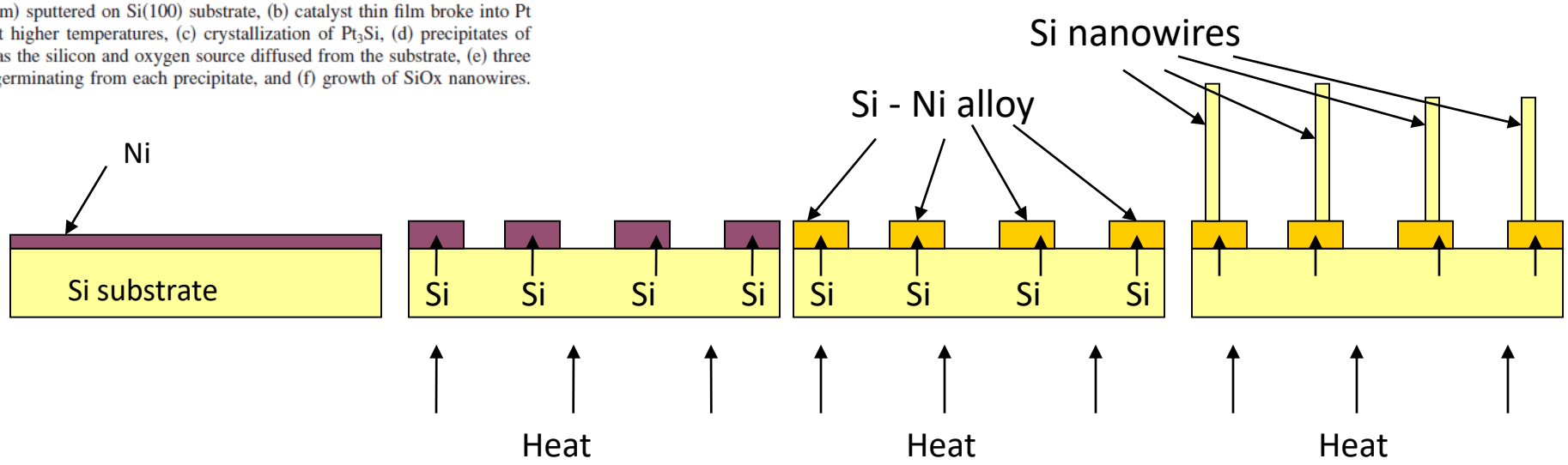


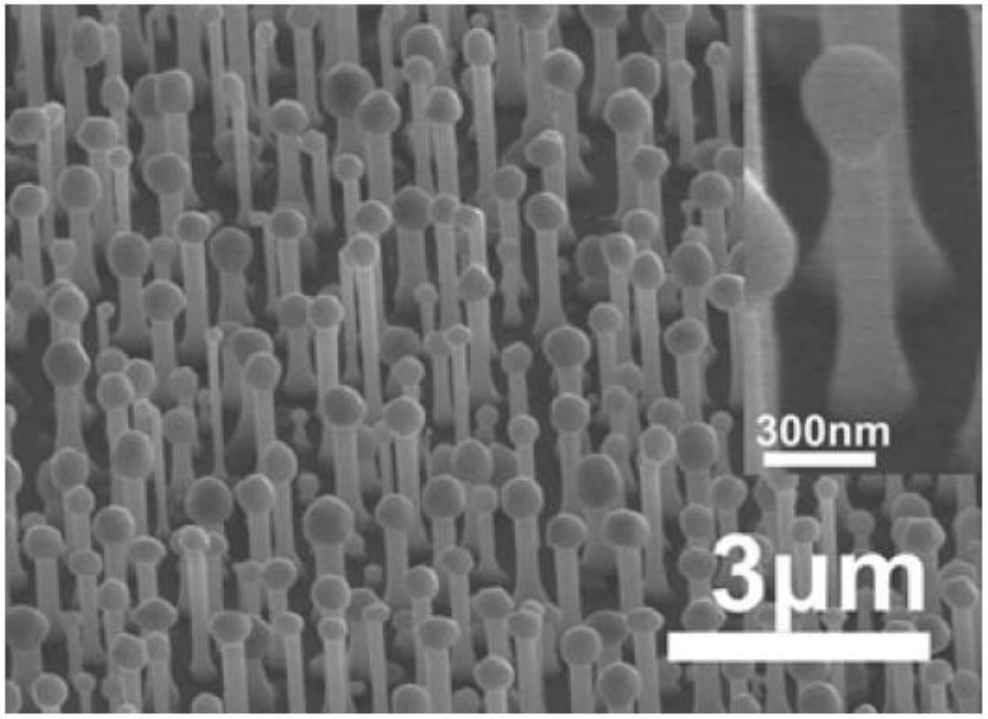

FIG. 5. Schematics of the SLS mechanism: (a) Pt catalyst thin film (~5 nm) sputtered on Si(100) substrate, (b) catalyst thin film broke into Pt dots at higher temperatures, (c) crystallization of $Pt_3Si$, (d) precipitates of SiOx as the silicon and oxygen source diffused from the substrate, (e) three buds germinating from each precipitate, and (f) growth of SiOx nanowires.




Ni coated Si substrate → Heat → diffusion of Si into Ni → Supersaturating of Ni




*H. J. Fan et al., Small 2 (2006) 700*

**VLS**

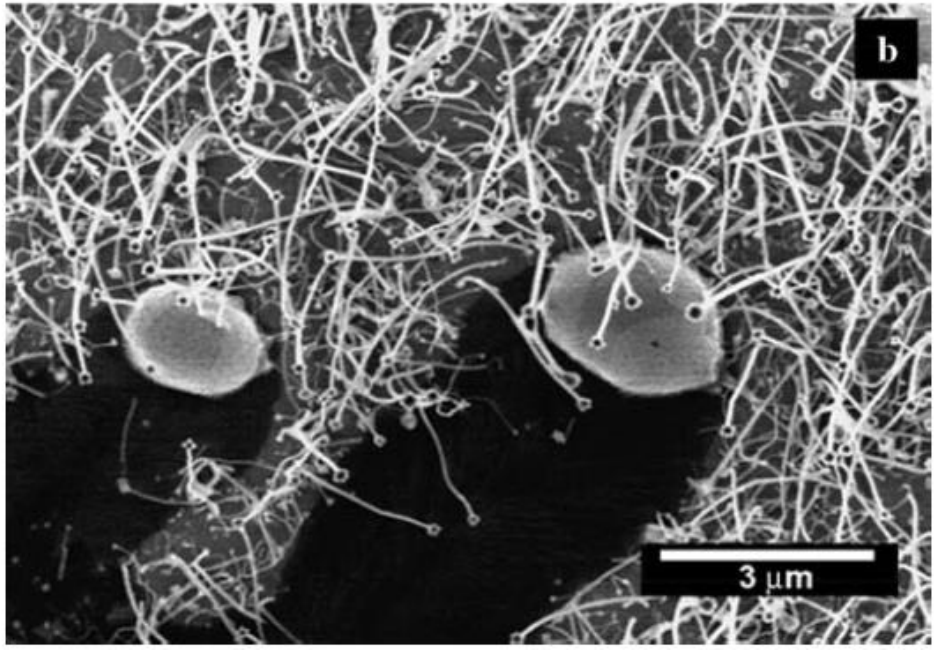
**SLS**

JOURNAL OF NANOSCIENCE AND NANOTECHNOLOGY

## Synthesis of Gold-Silica Composite Nanowires through Solid-Liquid-Solid Phase Growth

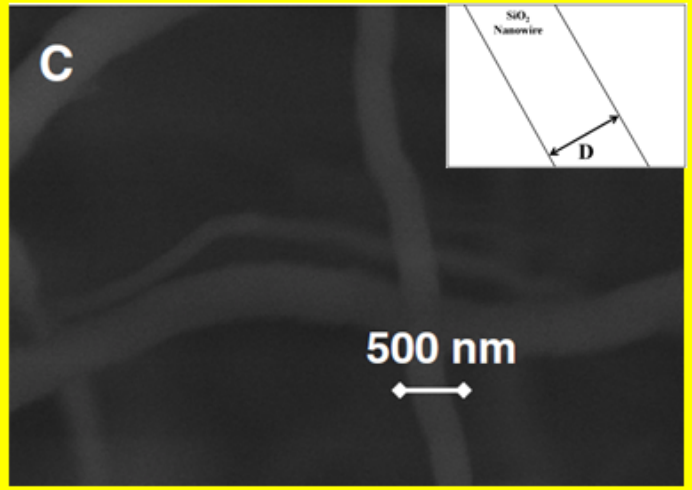
Maggie Paulose, Oomman K. Varghese, and Craig A. Grimes*

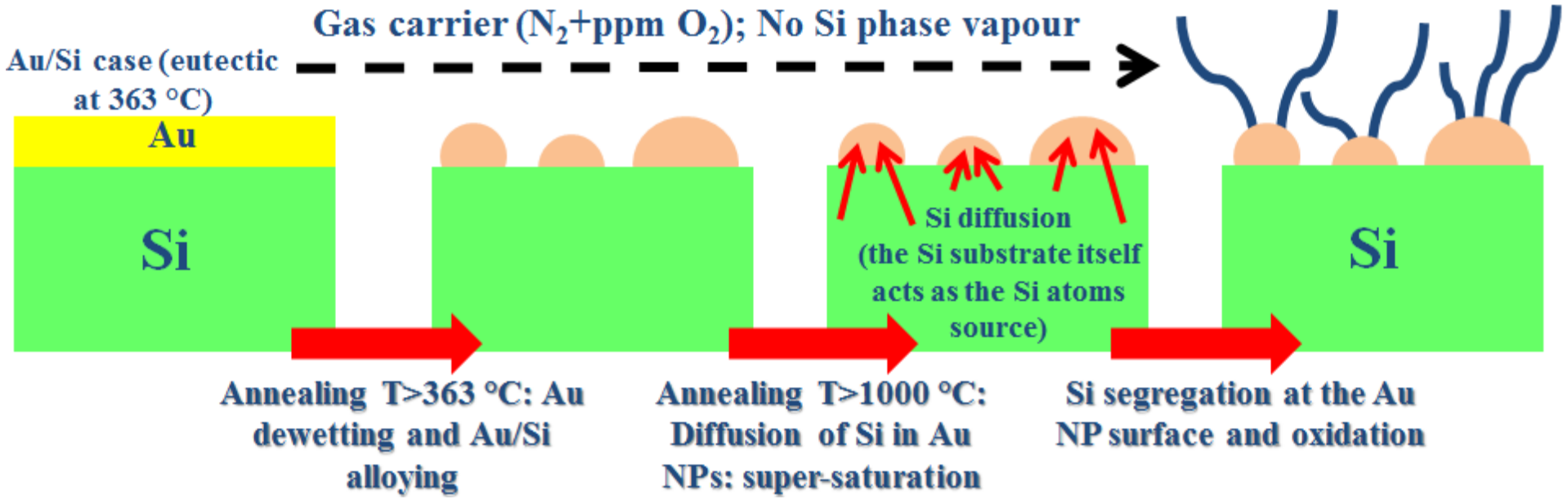
*J. L. Elechiguerra et al., Appl. Phys. A 79 (2004) 461*



# Metal-assisted growth without intentional Si phase vapor

**The main concern of the growth technique, towards reliable technological applications, is that the fabricated arrays consist of NWs with a very high diameter dispersion making practically impossible a fine control of the NWs size for specific applications.**

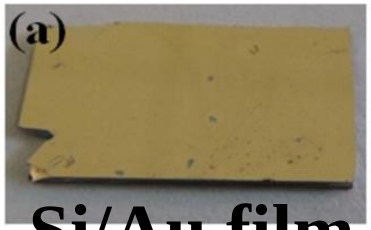



*M. Paulose et al., J. Nanosc. Nanotech. 3 (2003) 341; J. L. Elechiguerra et al. Appl. Phys. A 79 (2004) 461; P. K. Sekhar et al. Nanotechnology 17 (2006) 4606*

# Production of ultrathin size-selected $SiO_2$ NWs:

Experiments, Analysis, Results (F. Ruffino et al. Mater. Res. Express 2, 025003, 2015 )




1 cm

Si/Au film (gold)

h

Au film catalyst h=5, 10, 20, 30, 40, 80 nm

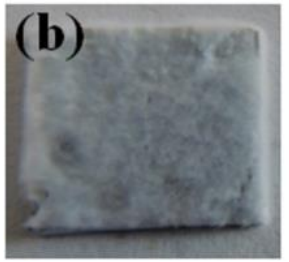
Si

$SiO_2$ NW growth

T=1100 °C, 1 h

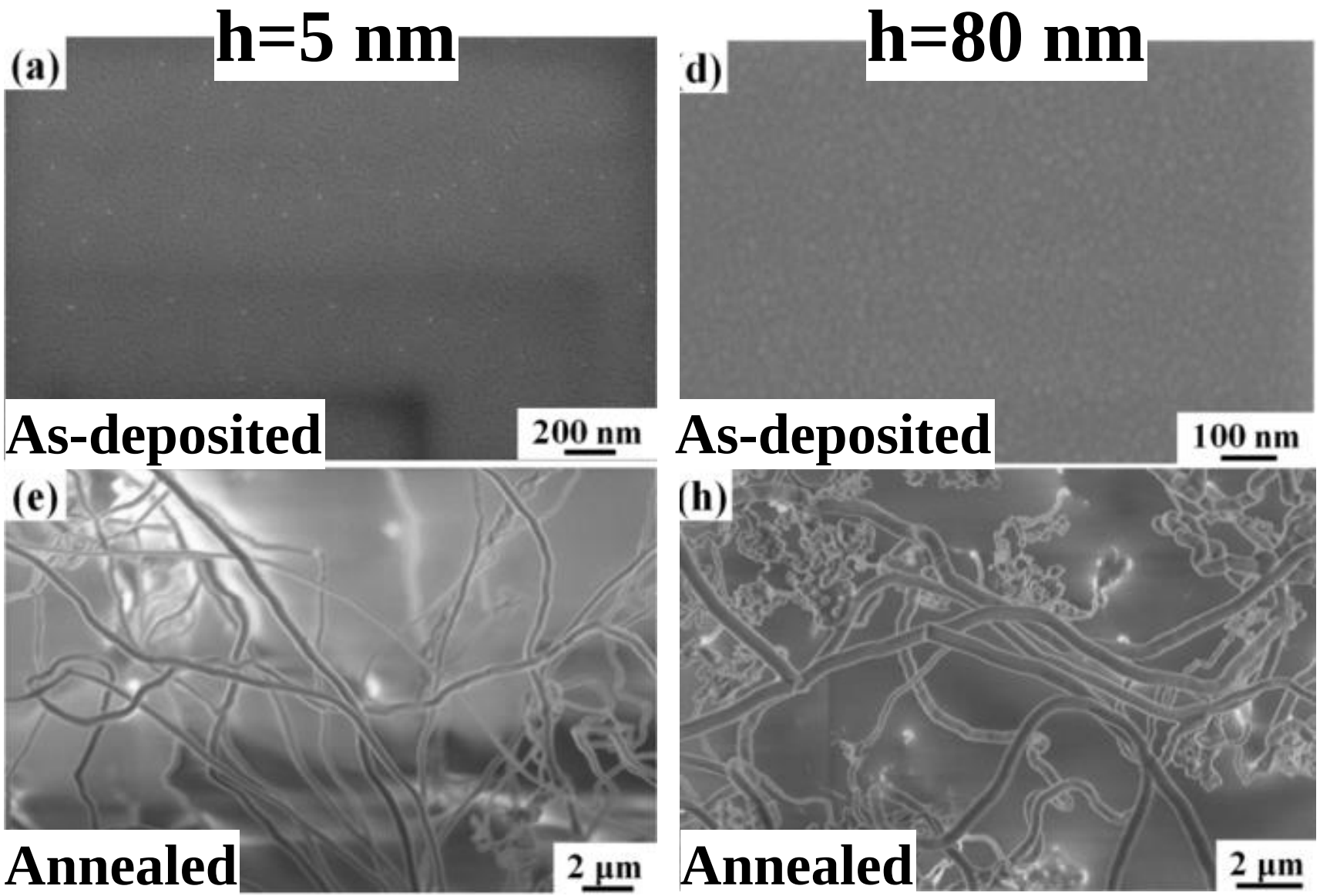
Si/$SiO_2$ NWs (white)

1 cm

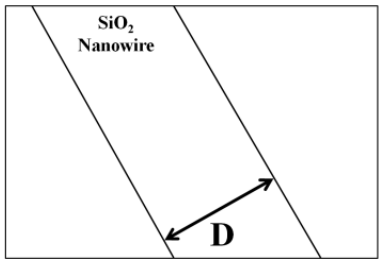


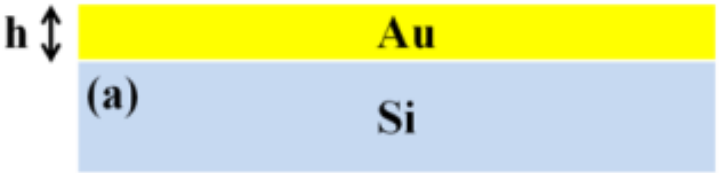

Si

## Experiment 1: $SiO_2$ NWs by Au films

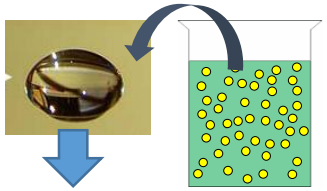

h=5 nm
h=80 nm
(a)
(d)
As-deposited
200 nm
As-deposited
100 nm
(e)
(h)
Annealed
2 µm
Annealed
2 µm

**SEM images**


SiO2
Nanowire
D


h
Au
(a)
Si

Solution drop rich in Au NPs



Si

Si/Au colloidal NPs (droplet spot)


1 cm

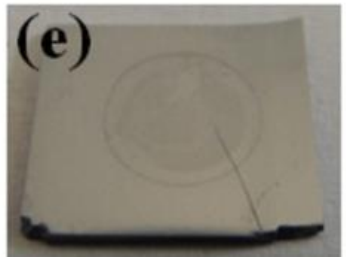
$d_0$=10, 30, 50, 80, 100 nm

Si

$SiO_2$ NW growth

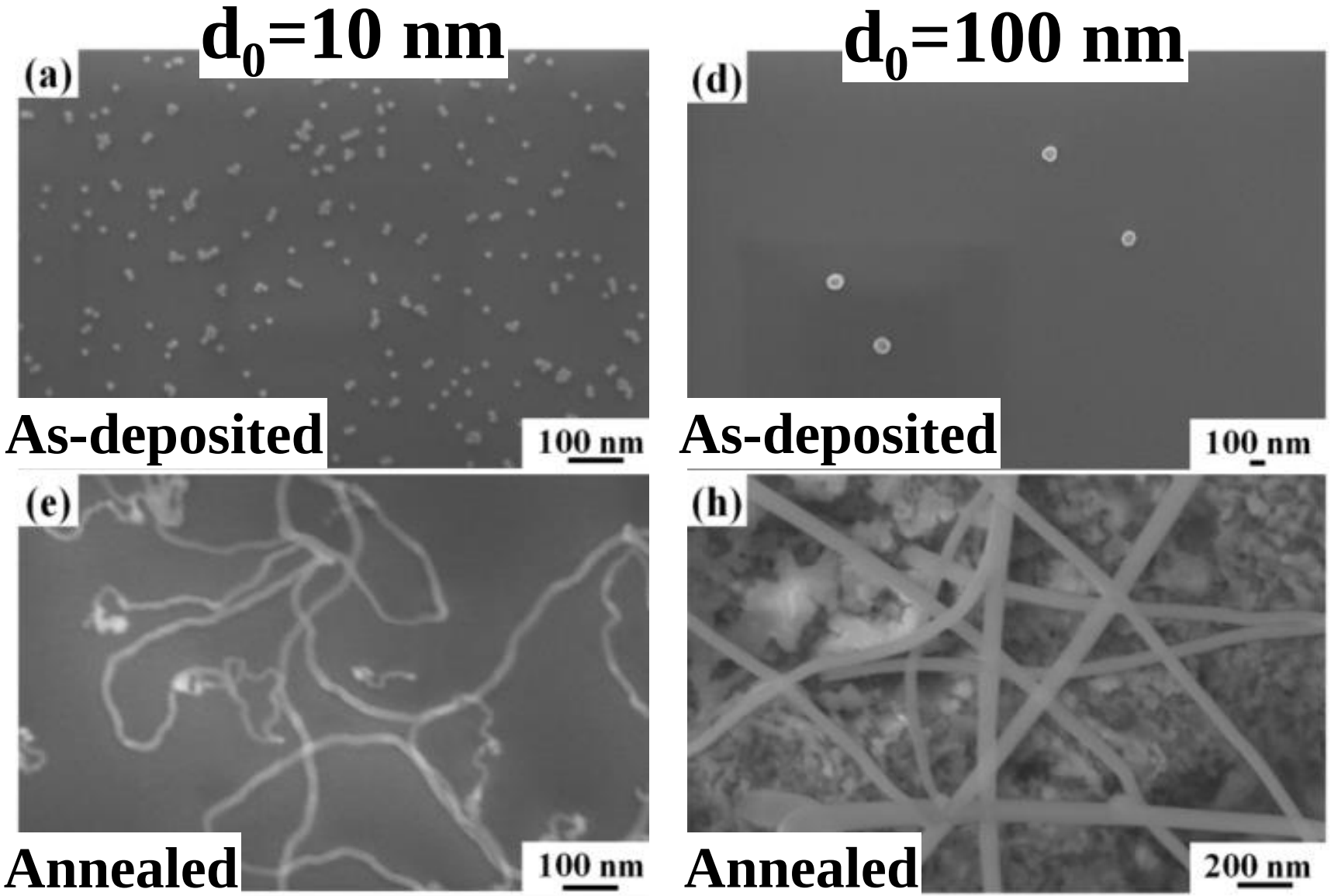
T=1100 °C, 1 h

1 cm

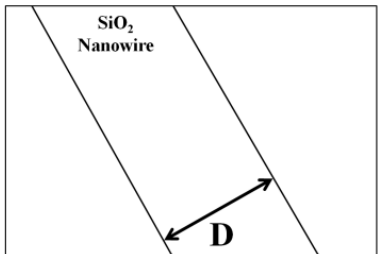



Si

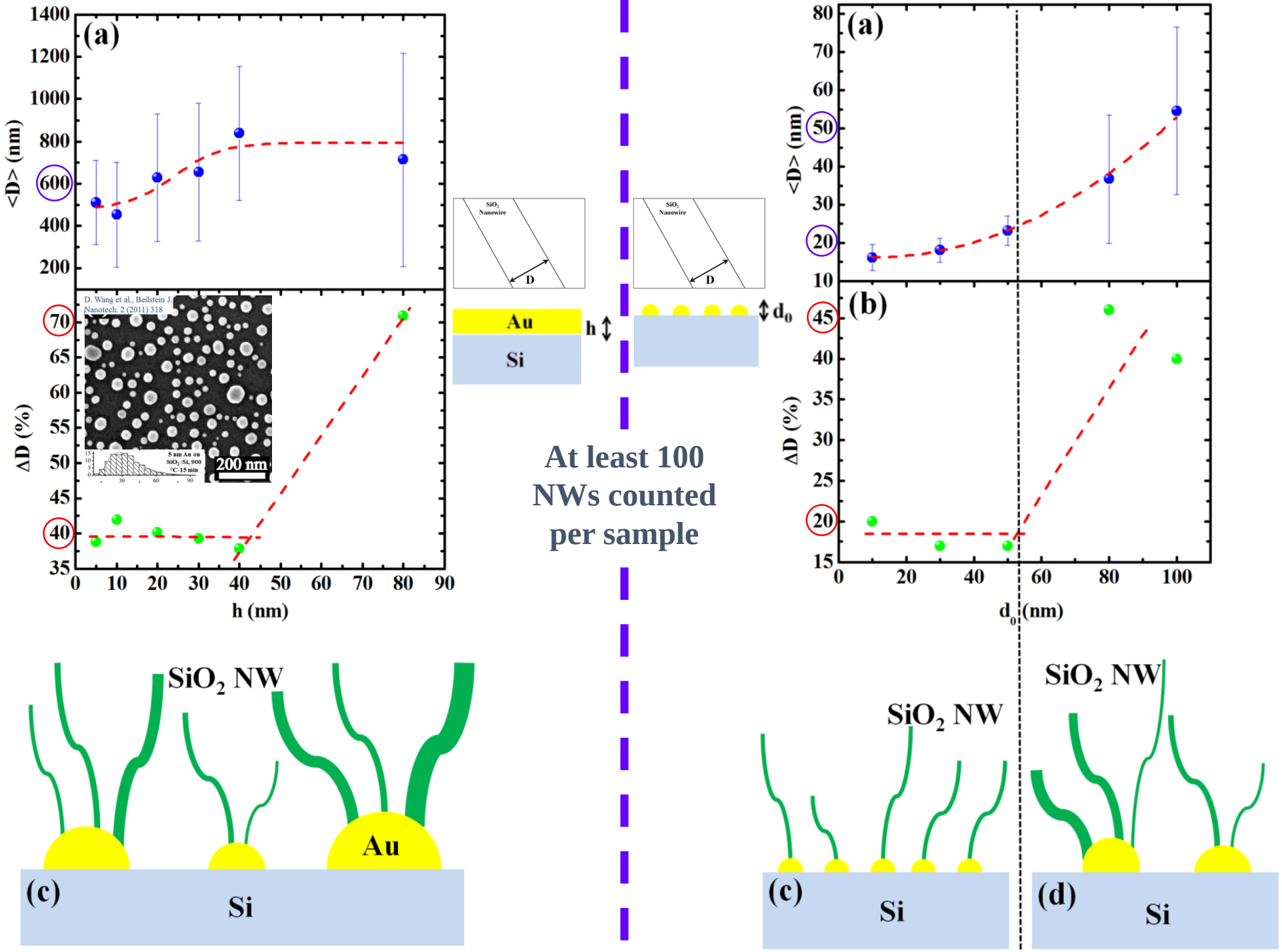
**Experiment 2: $SiO_2$ NWs by Au colloidal NPs**


$d_0$=10 nm
(a)
As-deposited
100 nm
$d_0$=100 nm
(d)
As-deposited
100 nm
(e)
Annealed
100 nm
(h)
Annealed
200 nm

**SEM images**


$SiO_2$
Nanowire
D


(e)
$d_0$

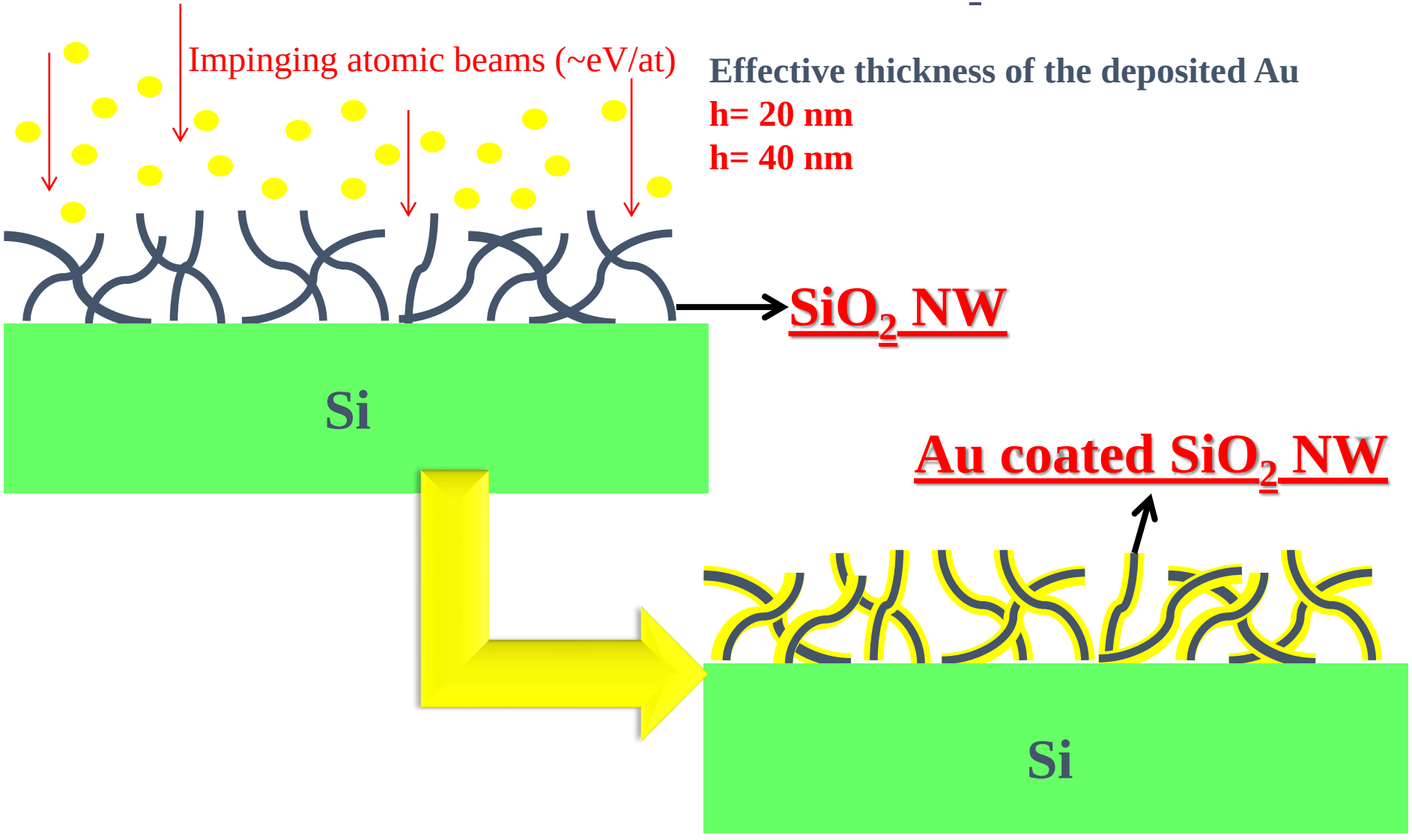

(a)
<D> (nm)
ΔD (%)
h (nm)
D. Wang et al., Beilstein J. Nanotech. 2 (2011) 318
200 nm
SiO2 Nanowire
D
Au
Si
h
d0
At least 100 NWs counted per sample
(a)
(b)
<D> (nm)
ΔD (%)
d0 (nm)
SiO2 NW
Au
(c)
Si
SiO2 NW
SiO2 NW
(c)
Si
(d)
Si

# Silica nanowires decorated by gold nanoparticles

# Production of Au NPs on silica NWs:

- **STEP 1: Au depositions to coat the nanowires (F. Ruffino et al. J. Nanopart. Res. 15, 1909, 2013; Physica E 69, 121, 2015)**

## Au depositions (sputtering) on the $SiO_2$ NWs

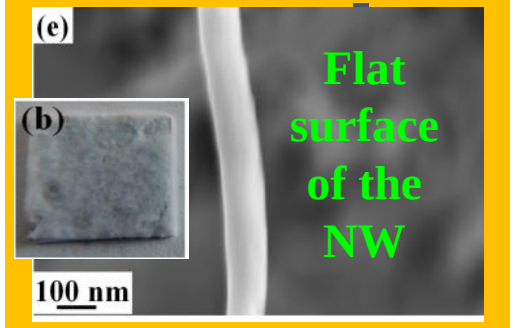



**Effective thickness of the deposited Au**

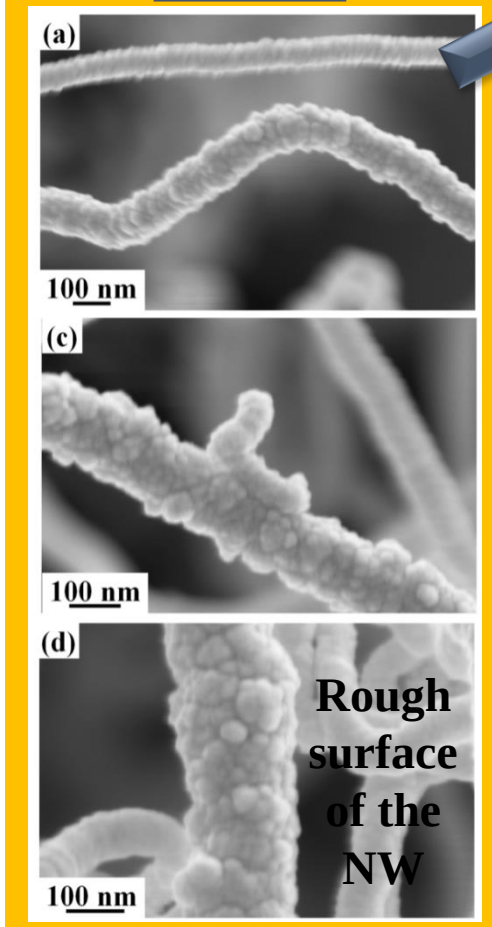
**h= 20 nm**

**h= 40 nm**

## As-grown $SiO_2$ NW

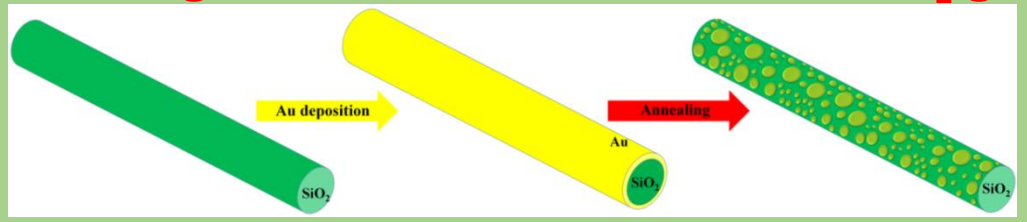



## After Au deposition h= 20 nm



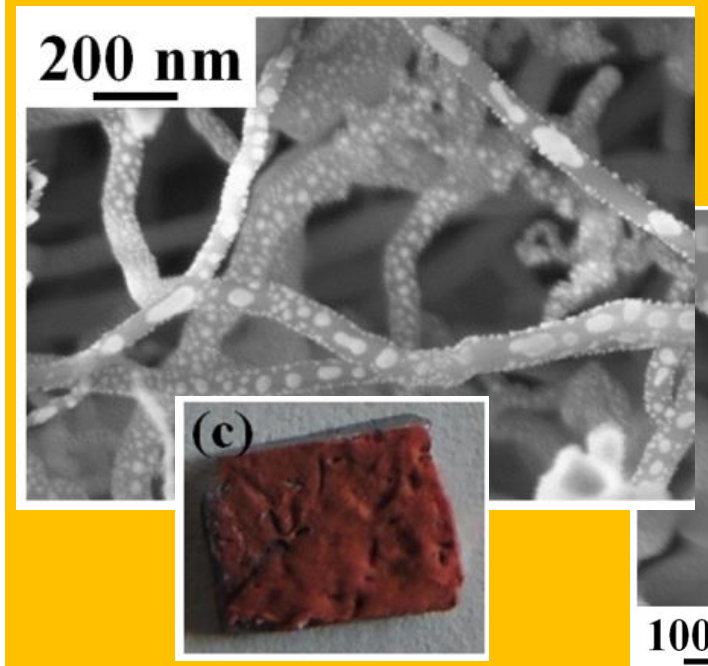

## Step 2: Annealing to induce a dewetting process

**Annealing: 700 °C, 800 °C, 900 °C-1h in $N_2$ gas**





## h= 20 nm, 700 °C-1h




**Well-defined NPs covering the NWs surface**